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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,493	12/11/2003	Yew Wee Cheong	42P17612	1630

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EXAMINER	
MCNALLY, DANIEL	

ART UNIT	PAPER NUMBER
1733	

DATE MAILED: 08/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/734,493	CHEONG ET AL.	
	Examiner	Art Unit	
	Daniel McNally	1733	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *20-22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-22* are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-19, drawn to methods for producing a flip chip assembly using a combination back grind tape and underfill, classified in class 156, subclass 153.

   II. Claims 20-22, drawn to a flip chip device, classified in class 257, subclass 778.

2. Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make another and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). Invention II is a device that can be manufactured by using the processes recited in Invention I. Specifically, Invention I recites applying a protective layer to a wafer before the wafer is separated into individual dice. Invention II can also be manufactured using an alternative process. A process comprising connecting a die, without a protective layer, to a substrate and injecting a protective layer between the die and substrate after they are already connected is an alternative to the methods of Invention I. It is evident that a process that is materially different from the processes of Invention I can produce Invention II.

3. Because these inventions are independent or distinct for the reasons given above and have acquired a separate status in the art in view of their different classification, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with Michael A. Bernadicou on August 15, 2006 a provisional election was made with traverse to prosecute the invention of the method, claims 1-19. Affirmation of this election must be made by applicant in replying to this Office action. Claims 20-22 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Specification

5. The disclosure is objected to because of the following informalities: "protective layer 102" in paragraph 0015 is labeled incorrectly. The protective layer should be labeled –302--

Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1, 4, 5, 8, 9,11-13,15 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Kumamoto [US-2003/0001283].

Kumamoto discloses a method of producing a chip assembly as broadly recited in claim 1. Kumamoto discloses the application of a coating 550' to a wafer 110, covering bumps 130 or "connection structures" (paragraph 0035). Note the discloser of a backgrinding process 350 (paragraph 0039), and the dicing of the wafer 800 into dice (paragraph 0042). Kumamoto also discloses connecting a die 800' to a substrate 960 (paragraph 0043), so the coating is between the die and the substrate as seen in Figure 13.

With regard to claim 4, Kumamoto discloses a solder-bumped wafer (paragraph 0022) comprising solder bumps 130 or "balls" as seen in Figure 1.

With regard to claim 5, Kumamoto discloses the application of heat to connect bumps 130 and lands 970 by solder flow (paragraph 0043).

Kumamoto discloses a method of dicing a wafer into dice as discussed with regard to claim 1. With regard to claim 8, Kumamoto also discloses a single die 800' being flipped together with its coating (paragraph 0042). Figure 9 shows the die and coating remains in contact.

Kumamoto discloses a method of producing a chip assembly as broadly recited in claim 9. Kumamoto discloses a wafer 110 with a circuit surface 120 adjacent to bumps 130 or "connection structures" (paragraph0022). Kumamoto discloses the application of a coating 550' to a wafer covering bumps (paragraph 0035). Note the discloser of a backgrinding process 350 (paragraph 0039), and the dicing of the wafer 800 into dice (paragraph 0042). Note the single die 800' is flipped together with its

coating 550' (paragraph 0042). Figure 9 shows the die is separated form the wafer without removing the coating.

With regard to claim 11, because the coating is not removed from the die, the coating and die remain in contact while they are separated into single pieces from the wafer.

Kumamoto discloses a method of producing a chip assembly as discussed with regard to claim 9. With regard to claim 12, Kumamoto also discloses connecting a die 800' to a substrate 960 (paragraph 0043), so the coating is between the die and the substrate as seen in Figure 13.

Kumamoto discloses a method of producing a chip assembly as broadly recited in claim 13. Kumamoto discloses the application of a coating 550' to a wafer 110, covering bumps 130 or "connection structures" (paragraph 0035). Note the discloser of dicing of the wafer 800 into dice (paragraph 0042). Kumamoto also discloses connecting a die 800' to a substrate 960 (paragraph 0043), so the coating is between the die and the substrate as seen in Figure 13.

With regard to claim 15, Kumamoto discloses a solder-bumped wafer (paragraph 0022) comprising solder bumps 130 or "balls" as seen in Figure 1.

With regard to claim 16, Kumamoto discloses the application of heat to connect bumps 130 and lands 970 by solder flow (paragraph 0043).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 2,3,6,7,10,14,17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumamoto in view of Nguyen et al. [US-6352881].

Kumamoto discloses a method of producing a chip assembly as discussed with regard to claim 1, in paragraph 7 above. Note Kumamoto discloses the coating 550' as a thermoset polymer in (paragraph 0036). Epoxy is a thermoset polymer but Kumamoto does not specifically disclose the use of epoxy, as recited in claim 2. Nguyen disclose a method of producing a flip chip assembly comprising a step of applying a layer of underfill adhesive 110 to a wafer 100 (column 3, lines 13-19). Nguyen teaches that the underfill can be epoxy based (column 4, lines 40-47). It would have been obvious to one of ordinary skill in the art at the time of invention to use an epoxy based material in Kumamoto's coating as taught by Nguyen in order to have an underfill material that will reduce the thermal stresses without reducing the thermal performance of the chip.

With respect to claim 3, Kumamoto does not disclose partially curing the coating after application. In Figure 11, it can be concluded that steps have been made to keep the coating from dripping off the die when the die and coating are flipped. Nguyen teaches a soft or pre-cure operation is performed to partially cure the underfill adhesive. It would have been obvious to one of ordinary skill in the art at the time of invention to partially cure Kumamoto's coating after application as taught by Nguyen in order to improve handling of the wafer.

Kumamoto discloses a method of producing a chip assembly as discussed with regard to claim 5, in paragraph 7 above. Note Kumamoto discloses the coating 550' as a thermoset polymer in (paragraph 0036). Epoxy is a thermoset polymer but Kumamoto does not specifically disclose the use and partial curing of epoxy, as recited in claim 6. Nguyen disclose a method of producing a flip chip assembly comprising a step of applying a layer of underfill adhesive 110 to a wafer 100 and around solder balls 108 (column 3, lines 13-19). Nguyen teaches that the underfill can be epoxy based (column 4, lines 40-47), and that it is partially cured after application. It would have been obvious to one of ordinary skill in the art at the time of invention to use an epoxy based material in Kumamoto's coating and to partially cure the coating after application as taught by Nguyen in order to have an easy to handle chip with an underfill material that will reduce the thermal stresses without reducing the thermal performance of the chip.

With respect to claim 7, Kumamoto discloses the application of heat to flow the solder bumps. Kumamoto does not disclose the heat also cures the coating. Nguyen teaches the application of heat causes the solder balls 108 to flow and finally cure the underfill adhesive. It would have been obvious to one of ordinary skill in the art at the time of invention to finish curing Kumamoto's coating as taught by Nguyen in order to create a strong bond between the die and substrate.

Kumamoto discloses a method of producing a chip assembly as discussed with regard to claim 9, in paragraph 7 above. Note Kumamoto discloses the coating 550' as a thermoset polymer in (paragraph 0036). Epoxy is a thermoset polymer but Kumamoto does not specifically disclose the use of epoxy, as recited in claim 10. Nguyen disclose

a method of producing a flip chip assembly comprising a step of applying a layer of underfill adhesive 110 to a wafer 100 and around solder balls 108 (column 3, lines 13-19). Nguyen teaches that the underfill can be epoxy based (column 4, lines 40-47). It would have been obvious to one of ordinary skill in the art at the time of invention to use an epoxy based material in Kumamoto's coating as taught by Nguyen in order to have an underfill material that will reduce the thermal stresses without reducing the thermal performance of the chip.

Kumamoto discloses a method of producing a chip assembly as discussed with regard to claim 13, in paragraph 7 above. Note Kumamoto discloses the coating 550' as a thermoset polymer in (paragraph 0036). Epoxy is a thermoset polymer but Kumamoto does not specifically disclose the use of epoxy, as recited in claim 14. Nguyen disclose a method of producing a flip chip assembly comprising a step of applying a layer of underfill adhesive 110 to a wafer 100 and around solder balls 108 (column 3, lines 13-19). Nguyen teaches that the underfill can be epoxy based (column 4, lines 40-47). It would have been obvious to one of ordinary skill in the art at the time of invention to use an epoxy based material in Kumamoto's coating as taught by Nguyen in order to have an underfill material that will reduce the thermal stresses without reducing the thermal performance of the chip.

Kumamoto discloses a method of producing a chip assembly as discussed with regard to claim 16, in paragraph 7 above. Note Kumamoto discloses the coating 550' as a thermoset polymer in (paragraph 0036). Epoxy is a thermoset polymer but Kumamoto does not specifically disclose the use and partial curing of epoxy, as recited

in claim 17. Nguyen disclose a method of producing a flip chip assembly comprising a step of applying a layer of underfill adhesive 110 to a wafer 100 and around solder balls 108 (column 3, lines 13-19). Nguyen teaches that the underfill can be epoxy based (column 4, lines 40-47), and that it is partially cured after application. It would have been obvious to one of ordinary skill in the art at the time of invention to use an epoxy based material in Kumamoto's coating and to partially cure the coating after application as taught by Nguyen in order to have an easy to handle chip with an underfill material that will reduce the thermal stresses without reducing the thermal performance of the chip.

Kumamoto discloses a method of producing a chip assembly comprising the application of a coating 550' to a wafer 110 with a circuit surface 120 adjacent to bumps 130 or "connection structures" (paragraph0022). Note the discloser of a backgrinding process 350 (paragraph 0039), and the dicing of the wafer 800 into dice (paragraph 0042). Kumamoto also discloses connecting a die 800' to a substrate 960 by using heat to connect bumps 130 and lands 970 by solder flow (paragraph 0043), so the coating is between the die and the substrate as seen in Figure 13. Kumamoto does not specifically disclose the use of epoxy in the coating, the partial curing of epoxy after application, and the final curing of the coating by heat during melting of the solder, as recited in claim 18. Nguyen disclose a method of producing a flip chip assembly comprising a step of applying a layer of underfill adhesive 110 to a wafer 100 and around solder balls 108 (column 3, lines 13-19). Nguyen teaches that the underfill can be epoxy based (column 4, lines 40-47), that it is partially cured after application and the heat applied to melt the solder balls 108 will cure the underfill adhesive. It would have

been obvious to one of ordinary skill in the art at the time of invention to use an epoxy based material in Kumamoto's coating, to partially cure the coating after application and to finish curing the coating as taught by Nguyen in order to have an easy to handle chip with an underfill material that will reduce the thermal stresses without reducing the thermal performance of the chip.

10. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kumamoto in view of Nguyen et al. as applied to claims 2,3,6,7,10,14,17 and 18 above, and further in view of White [US-5535526].

Kumamoto, as modified, discloses a method of producing a chip assembly as discussed with regard to claim 18, in paragraph 9 above. Kumamoto does not disclose coupling the substrate to a circuit board. White teaches a method of mounting a substrate 404 on a circuit board 416 (column 7, lines 24-45). White also discloses a flip chip 402 connected to the substrate by solder joints 406 and an encapsulant 408 or "protective layer" between the flip chip and substrate. It would have been obvious to one of ordinary skill in the art at the time of invention to connect Kumamoto's chip assembly to a circuit board as taught by White in order to expand the capabilities of the chip.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Grigg et al. [US-6506681] discloses a method of producing a flip chip assembly comprising the use of a molding compound that serves as protection during dicing.

Satoh [US-6338980] discloses a method of producing a chip assembly comprising the use of a protective resin during grinding and dicing.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel McNally whose telephone number is (571) 272-2685. The examiner can normally be reached on Monday - Friday 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Crispino can be reached on (571)272-1226. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Daniel McNally
Examiner
Art Unit 1733

dpm
August 16, 2006

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